

LV52130A0XA LV52130A4XA



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Advance Information

Bi-CMOS IC

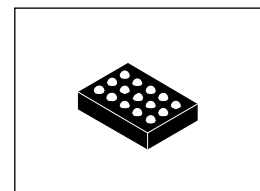
1coil Boost DC-DC converter and Inverter Charge Pump

Overview

The LV52130A0XA and LV52130A4XA are dual-output with 1coil boost DC-DC converter and built-in inverter charge pump circuit.

Function

- 1 coil Dual-outputs
- VOUT1 output (+5V/+5.4V)
- VOUT2 output (-5V/-5.4V)
- Operating Voltage from 2.5V to 5.5V
- Each output voltages adjusted by I2C (I2C disable at standby)
- Synchronous Rectification
- SCP(VOUT1 to gnd / VOUT2 to gnd)
- Standby current dissipation 0.3μA



WLP15 - 0.4mm pitch
(1.55mm × 2.15mm, Amax=0.625mm)

Typical Applications

LCD / AMOLED panel power supply

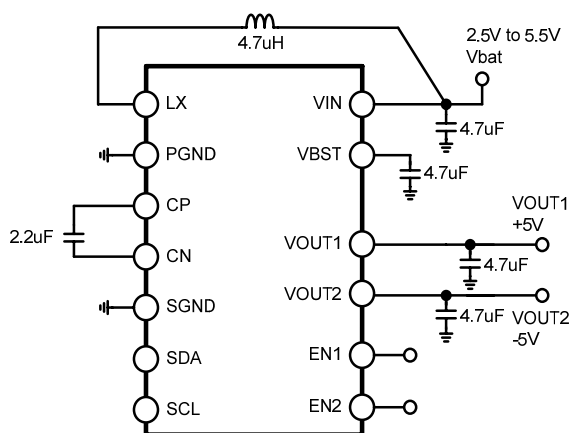


Fig.1 Application

* I²C Bus is a trademark of Philips Corporation.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

LV52130A0XA/4XA

Specifications

LV52130A0XA DEFAULT: VOUT1=+5V, VOUT2=-5V
MARKING: 130A0 YMXX

LV52130A4XA DEFAULT: VOUT1=+5.4V, VOUT2=-5.4V
MARKING: 130A4 YMXX

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VINmax	VIN to GNDs	+6	V
Maximum Pin voltage1	Vpin1max	CN,VOUT2 to GNDs	-6	V
Maximum Pin voltage2	Vpin2max	LX	+7	V
Maximum Pin voltage3	Vpin3max	Other pin to GNDs	+6	V
Allowable power dissipation	Pdmax	Ta=25°C The specified board*1	1	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

*1 Mounted on a specified board: 50mm×50mm×1mm (2 layer glass epoxy)

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VIN op	VIN	2.5 to 5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics

at Ta = 25°C, PVIN=VIN=3.7V VOUT1=5V VOUT2=-5V (Unless otherwise noted)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VIN current						
Standby current dissipation	ICC1	IC disable		0.3		uA
VBST DCDC Converter						
VBST current limit	ICLBST	LX	0.9	1.2	1.5	A
VOUT1 LDO						
VOUT1 voltage	VOUT1	Default		5		V
VOUT1 voltage range	VOUT1	100mVsteps by I2C	4.1		5.7	V
VOUT1 voltage accuracy	VOUT1		-1		1	%
VOUT1 dropout voltage	Vdrop	150mA		150		mV
VOUT1 current	IOUT1	IOUT2=0			200	mA
VOUT1 line regulation	VLINR1	dVo=1V Io=30mA		0.3		%/V
VOUT1 load regulation	VLDR1	Io=2mA/150mA		4		mV
Discharge Resistance 1	RVO1			70		Ω
Soft-start	tssv01			0.2		ms

Continued on next page

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Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VOUT2 Charge pump						
VOUT2 voltage	VOUT2	Default		-5		V
VOUT2 voltage range	VOUT2R	100mV steps by I2C	-5.7		-4.1	V
VOUT2 voltage accuracy	VOUT2A		-1		1	%
VOUT2 current	IOUT2	IOUT1=0			100	mA
VOUT2 line regulation	VLINR2	dVo=1V Io=30mA		0.3		%/V
VOUT2 load regulation	VLDR2	Io=2mA/60mA		20		mV
Discharge Resistance 2	RVO2			20		Ω
Soft-start	tssvo2			0.2		ms
OSC						
OSC frequency1	Fosc1	Boost-DCDC	1.48	1.85	2.22	MHz
OSC frequency2	Fosc2	charge pump	0.74	0.925	1.11	MHz
ULVO						
UVLO up	Vuvlo_h	VIN up			2.5	V
UVLO down	Vuvlo_l	VIN down			2.3	V
Control Input						
High level input voltage	VINH	SDA/SCL/EN1/EN2	1.26		VIN	V
Low level input voltage	VINL	SDA/SCL/EN1/EN2	0		0.54	V
Pulldown Resistance	Rpd	EN1/EN2		400		kΩ

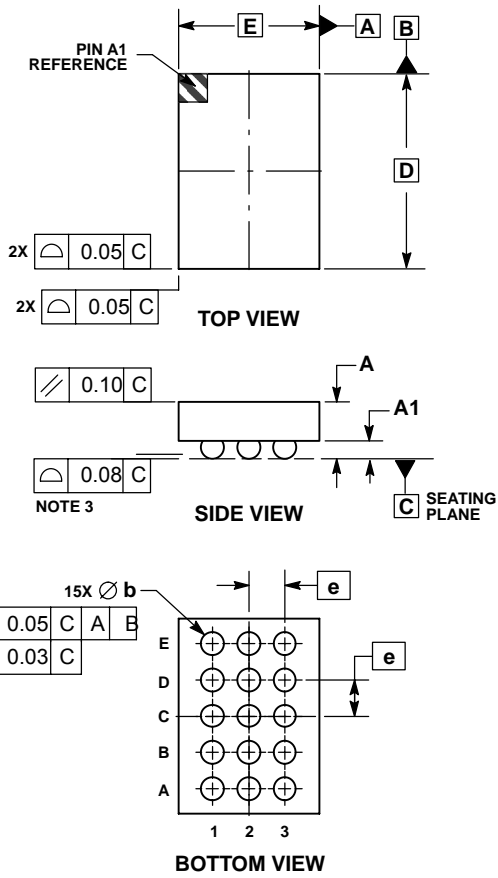
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LV52130A0XA/4XA

Package Dimensions

unit : mm

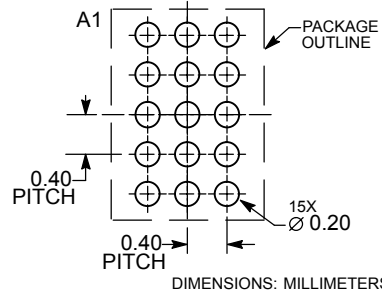
WLCSP15, 2.15x1.55
CASE 567HY
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.625
A1	0.16	0.26
b	0.20	0.30
D	2.15 BSC	
E	1.55 BSC	
e	0.40 BSC	

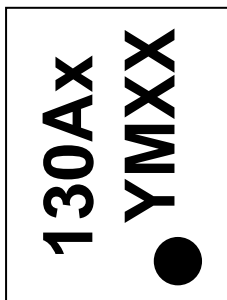
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LV52130A0XA/LV52130A4XA is as follows.

MARKING DIAGRAM
Top view



- = Device Mark
- XX = Assembly lot Code (Tentative)

LV52130A0XA/4XA

Block Diagram

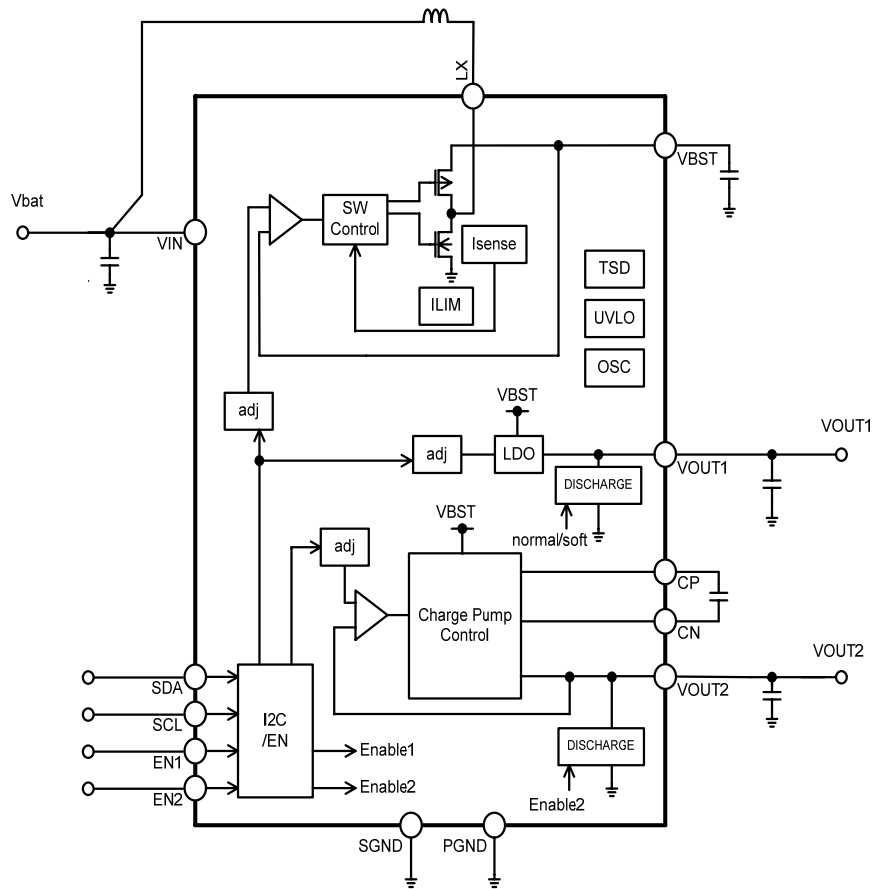
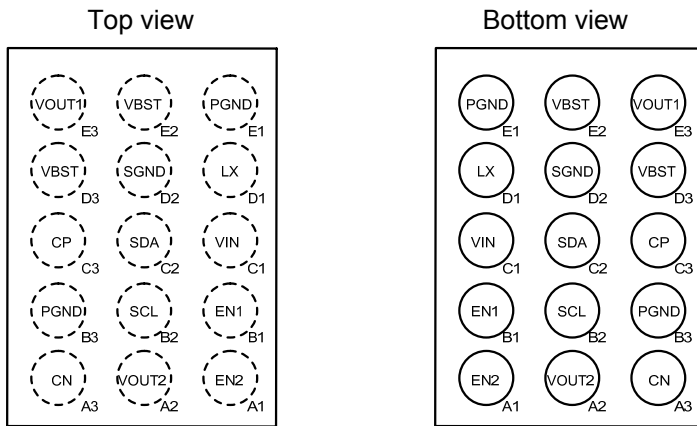


Fig.2 Block Diagram

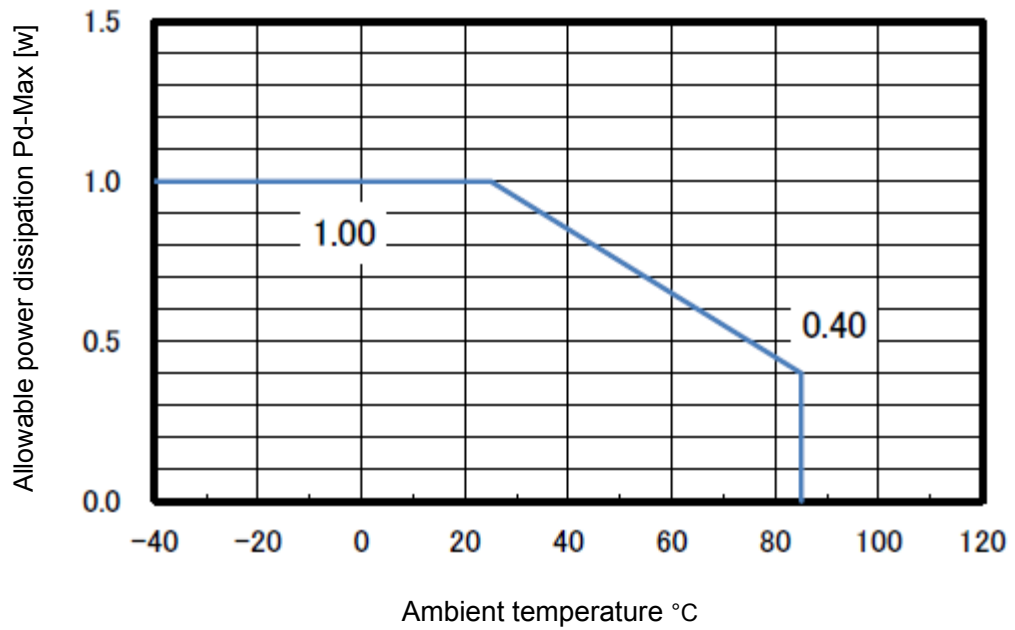
Pin Function

PIN #	Pin Name	Description
A1	EN2	Enable1 input pin
A2	VOUT2	VOUT2 output pin
A3	CN	Flying capacitor connection pin for charge pump
B1	EN1	Enable1 input pin
B2	SCL	I2C clock signal input pin
B3/E1	PGND	Power Ground
C1	VIN	Power supply voltage
C2	SDA	I2C data signal input / output pin
C3	CP	Flying capacitor connection pin for charge pump
D1	LX	Boost converter switching pin
D2	SGND	Signal Ground
D3/E2	VBST	Boost converter direct output pin
E3	VOUT1	VOUT1 output pin

PIN CONNECTIONS



Pd-Max



Mounted on a specified board: 50mm×50mm×1mm (2 layer glass epoxy)

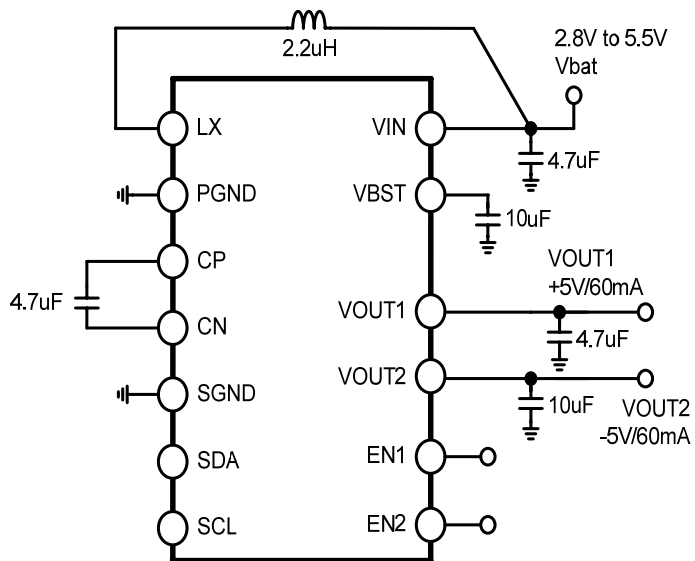
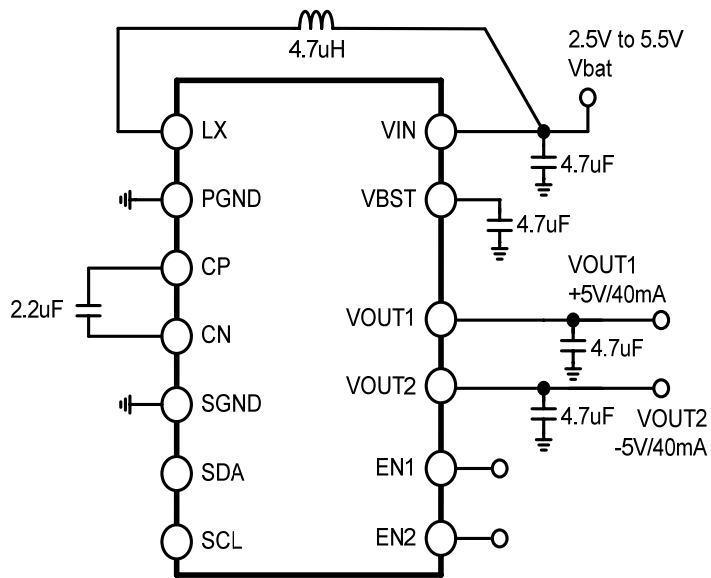


Fig.3 Recommendation Applications

Table . Component List for Typical Characteristics Circuit

Reference	Description	Manufacturer and Part Number
C	2.2uF, +-10%, 10V, X5R, ceramic	TDK - C1608X5R1A225K
	4.7uF, +-10%, 10V, X5R, ceramic	TDK - C1608X5R1A475K
	10uF, +-10%, 10V, X5R, ceramic	TDK - C1608X5R1A106K
L	2.2uH, 1.1A, 120mohm, 2.5mm*2.0mm*1.1mm	TDK – MLP2520V2R2ST0S1
	4.7uH, 0.8A, 220mohm, 2.5mm*2.0mm*1.1mm	TDK – MLP2520V4R7ST0S1

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BITMAP (I2C control) / I2C disable at standby

WRITE: IC Address : 0111110x x=0:Write mode / x=1:inhibition

	Sub Address	MSB							LSB
		(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
VOUT1	0000 0000	-	-	-	VOUT1	VOUT1	VOUT1	VOUT1	VOUT1
VOUT2	0000 0001	-	-	-	VOUT2	VOUT2	VOUT2	VOUT2	VOUT2
Mode	0000 0011							XDIS1	XDIS2

bits	VOUT1 [V]	VOUT2 [V]
0	not use	not use
1	4.1	-4.1
2	4.2	-4.2
3	4.3	-4.3
4	4.4	-4.4
5	4.5	-4.5
6	4.6	-4.6
7	4.7	-4.7
8	4.8	-4.8
9	4.9	-4.9
10	5.0*	-5.0*
11	5.1	-5.1
12	5.2	-5.2
13	5.3	-5.3
14	5.4**	-5.4**
15	5.5	-5.5
16	5.6	-5.6
17	5.7	-5.7

* :default = +-5V (LV52130A0XA)

** :default = +-5.4V (LV52130A4XA)

XDIS1=1 :VOUT1 discharge enable(default), XDIS1=0 :VOUT1 discharge disable

XDIS2=1 :VOUT2 discharge enable(default), XDIS2=0 :VOUT2 discharge disable

LV52130A0XA/4XA

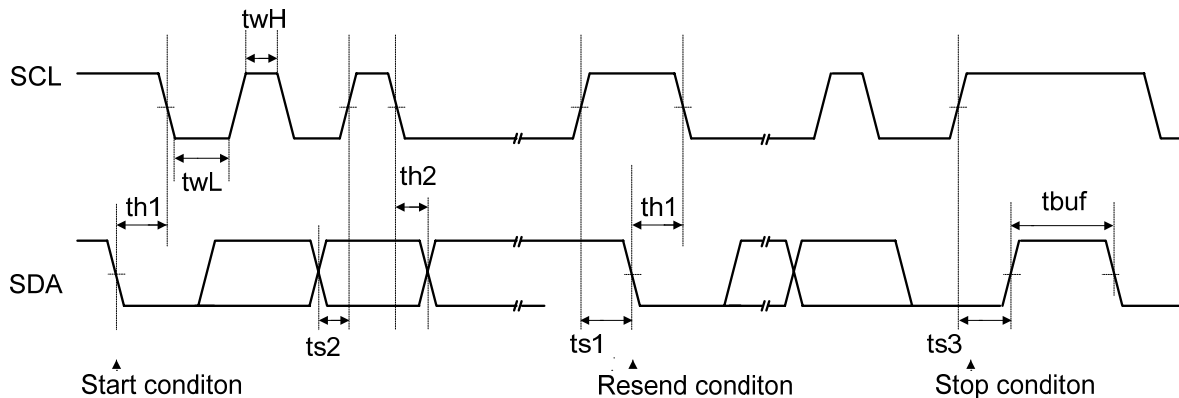
Serial Bus Communication Specifications Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	100	kHz
Data set up time	ts1	SCL setup time relative to the fall of SDA	4.7	-	-	us
	ts2	SDA setup time relative to the rise of SCL	250	-	-	ns
	ts3	SCL setup time relative to the rise of SDA	4.0	-	-	us
Data hold time	th1	SCL data hold time relative to the rise of SDA	4.0	-	-	us
	th2	SDA hold time relative to the fall of SCL	0	-	-	us
Pulse width	twL	SCL pulse width for the L period	4.7	-	-	us
	twH	SCL pulse width for the H period	4.0	-	-	us
Input waveform conditions	ton	SCL and SDA (input) rise time	-	-	1000	ns
	tof	SCL and SDA (input) fall time	-	-	300	ns
Bus free time	tbuf	Time between STOP and START conditions	4.7	-	-	us

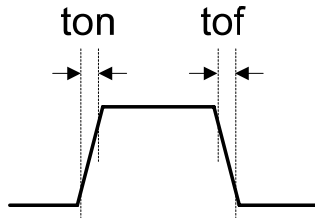
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	400	kHz
Data setup time	ts1	SCL setup time relative to the fall of SDA	0.6	-	-	us
	ts2	SDA setup time relative to the rise of SCL	100	-	-	ns
	ts3	SCL setup time relative to the rise of SDA	0.6	-	-	us
Data hold time	th1	SCL data hold time relative to the rise of SDA	0.6	-	-	us
	th2	SDA hold time relative to the fall of SCL	0	-	-	us
Pulse width	twL	SCL pulse width for the L period	1.3	-	-	us
	twH	SCL pulse width for the H period	0.6	-	-	us
Input waveform conditions	ton	SCL and SDA (input) rise time	-	-	300	ns
	tof	SCL and SDA (input) fall time	-	-	300	ns
Bus free time	tbuf	Time between STOP and START conditions	1.3	-	-	us

I²C serial transfer timing conditions

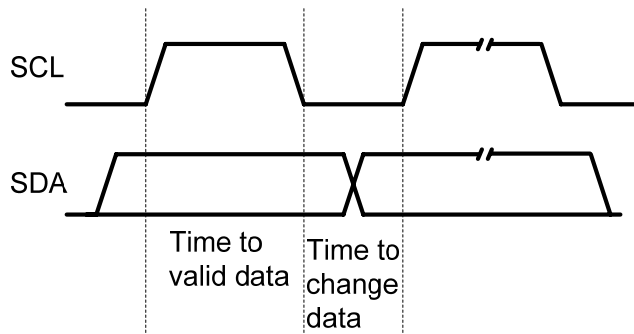


Input waveform condition

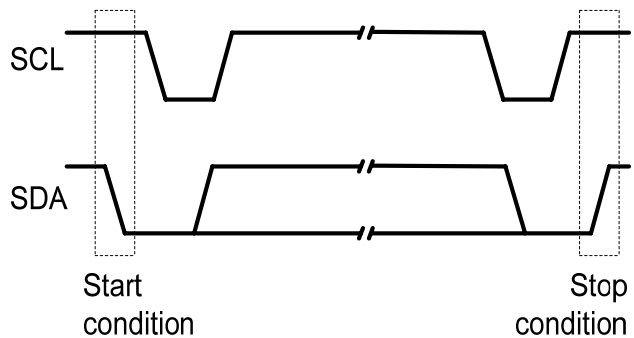


I2C control transmission method

In start and stop conditions of the I²C bus, SDA should be kept in the constant state while SCL is "H" as shown below during data transfer.



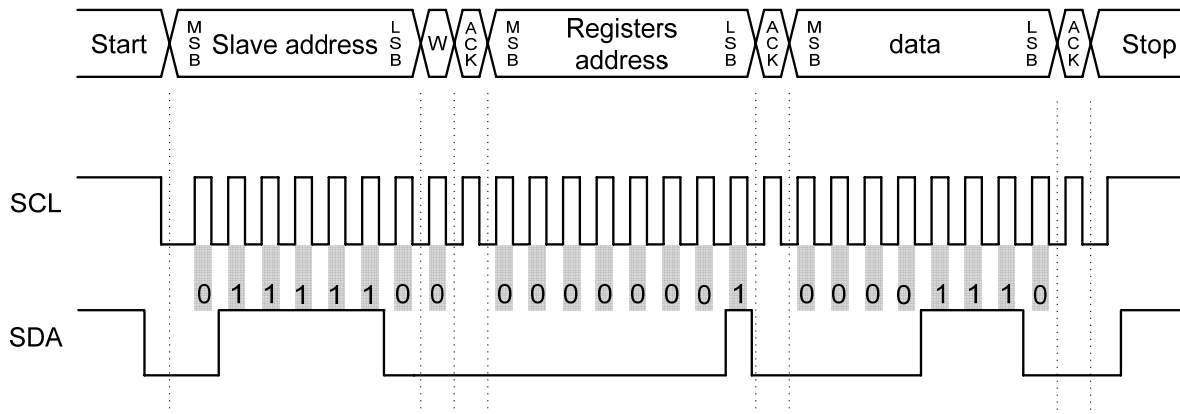
When data transfer is not made, both SCL and SDA are in the "H" state.
 When SCL = SDA="H", change of SDA from "H" to "L" enables the start conditions to start access.
 When SCL is "H", change of SDA from "L" to "H" enables the stop conditions to stop access.



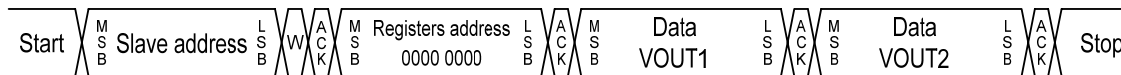
Data transfer and acknowledgement response

After establishment of start conditions, Data transfer is made by one byte (8 bits). Data transfer enables continuous transfer of any number of bytes. Each time of the 8-bit data is transferred, the ACK signal is sent from the receive side to the send side. The ACK signal is issued when SDA(on the send side) is released and SDA(on the receive side) is set "L" immediately after fall of the clock pulse at the SCL eighth bit of data transfer to "L". When the next 1-byte transfer is left in the receive state after transmission of the ACK signal from the receive side, the receive side releases SDA at fall of the SCL ninth clock. In the I2C bus, there is no CE signal. Instead, 7-bit slave address is assigned to each device and the first byte of transfer is assigned to the command (R/W) representing the 7-bit slave address and subsequent transfer direction. Note that only WRITE is valid in this IC. The 7-bit address is transferred sequentially from MSB and the eighth bit is "L" representing WRITE.

Input 1 data



Input 2 data (register address auto Increment)



Detailed Descriptions

The LV52130Ax has dual-output VOUT1 (LDO) and VOUT2 (built-in inverter charge pump) with 1coil boost dcdc converter. Both outputs are separately controlled by I2C control and pin EN1/EN2. Boost converter is a fixed-frequency pulse width modulated (PWM) regulator. At rated load, each converter operates at continuous conduction mode (CCM). At light loads, both converters can enter in discontinuous conduction mode (DCM). Cycle-by-cycle peak current limit and thermal provide value added features to protect the device.

Start Sequencing

Enable input (pin EN1/EN1) is used as enable input logic. An active high logic level on this pin enables the device. A built-in pull-down resistor disables the device if the pin is left open. If a high logic signal is applied, the LV52130Ax starts with timing sequence as depicted Figure 4 (Case1/Case2).

It must be set ($5.4V \geq V_{OUT1} \text{ bit} / V_{OUT2} \text{ bit} \geq -5.4V$) and ($V_{OUT1} \text{ current} < 100mA$) at start sequencing.

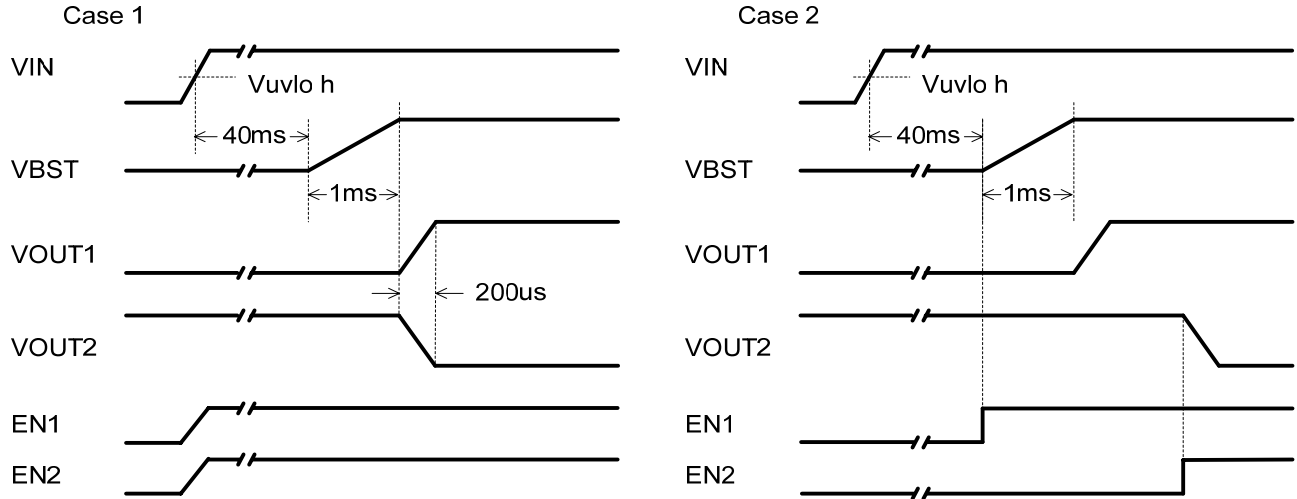


Fig.4 Sequencing Diagram

Inductor Selection

Three different electrical parameters need to be considered when selecting an inductor, the value of the inductor, the saturation current and the DCR. During normal and heavy load operation, the LV52130Ax is intended to operate in Continuous Conduction Mode (CCM). The equation below can be used to calculate the peak current.

$$I_{peak_p} = I_{out1} / (n1 \times (1 - D1)) + (VIN \times D1) / 2 \times L1 \times Fosc1$$

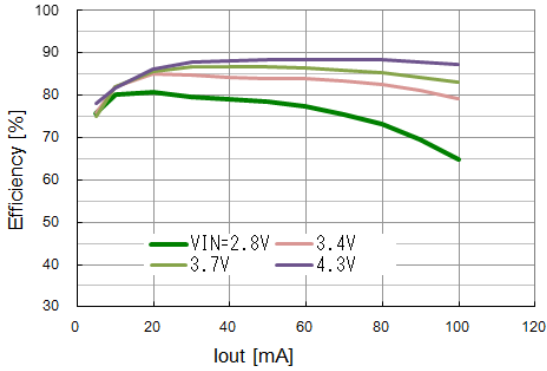
VIN:battery voltage, IOUT1:load current, L:inductor value, Fosc1: OSC frequency1, D1:duty cycle, n1:converter efficiency varies with load current.

A good approximation is to use $\eta = 0.85$. It is important to ensure that the inductor current rating is high enough such that it not saturate. As the inductor size is reduced, the peak current for a given set of conditions increases along with higher current ripple so it is not possible to deliver maximum output power at lower inductor values. Finally an acceptable DCR must be selected regarding losses in the coil and must be lower than 250 mΩ (typical) to limit excessive voltage drop. In addition, as DCR is reduced, overall efficiency will improve. The inductor value is recommended to use a 4.7 uH or 2.2uH.

TYPICAL OPERATING CHARACTERISTICS

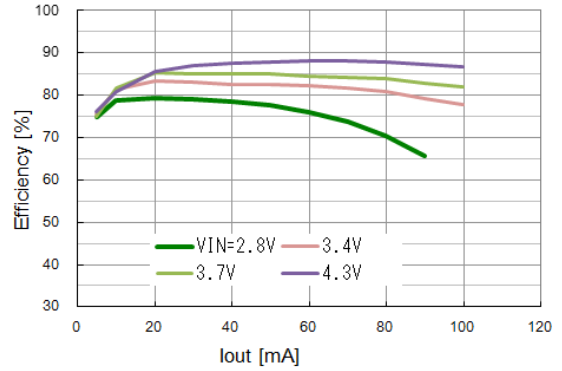
Efficiency

VOUT1=5V, VOUT2=-5V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=4.7uF, C_{bst}=4.7uF,
 C_{cp_cn}=2.2uF, C_{vin}=10uF+4.7uF, L=4.7uH



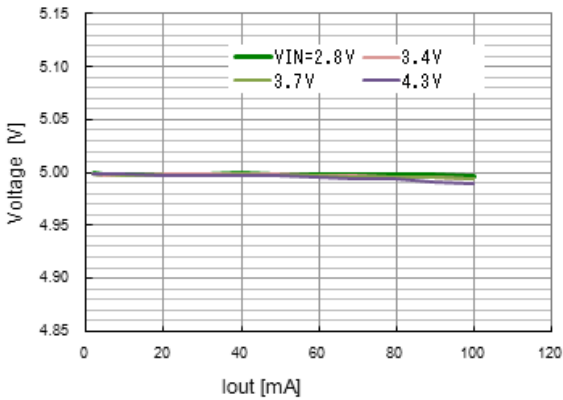
Efficiency

VOUT1=5.4V, VOUT2=-5.4V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=4.7uF, C_{bst}=4.7uF,
 C_{cp_cn}=2.2uF, C_{vin}=10uF+4.7uF, L=4.7uH



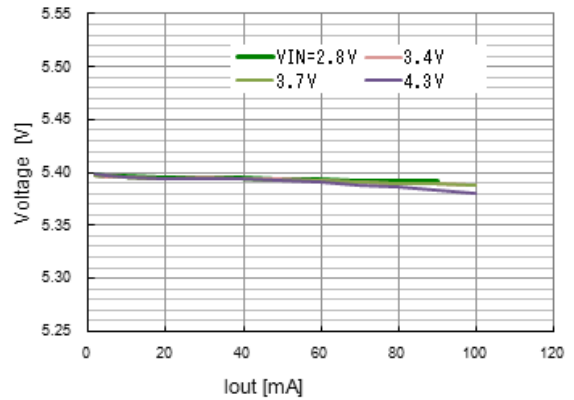
Load Regulation VOUT1

VOUT1=5V, VOUT2=-5V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=4.7uF, C_{bst}=4.7uF,
 C_{cp_cn}=2.2uF, C_{vin}=10uF+4.7uF, L=4.7uH



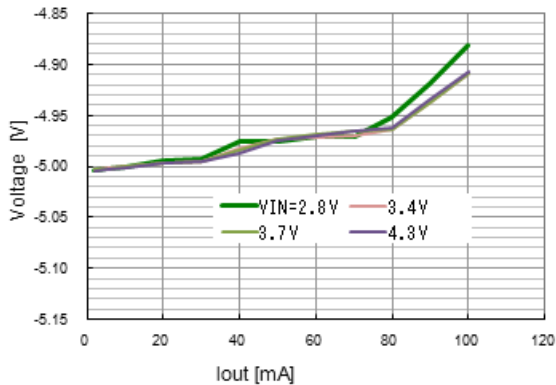
Load Regulation VOUT1

VOUT1=5.4V, VOUT2=-5.4V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=4.7uF, C_{bst}=4.7uF,
 C_{cp_cn}=2.2uF, C_{vin}=10uF+4.7uF, L=4.7uH



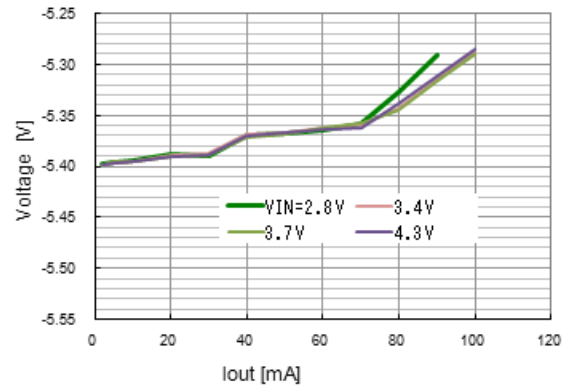
Load Regulation VOUT2

VOUT1=5V, VOUT2=-5V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=4.7uF, C_{bst}=4.7uF,
 C_{cp_cn}=2.2uF, C_{vin}=10uF+4.7uF, L=4.7uH



Load Regulation VOUT2

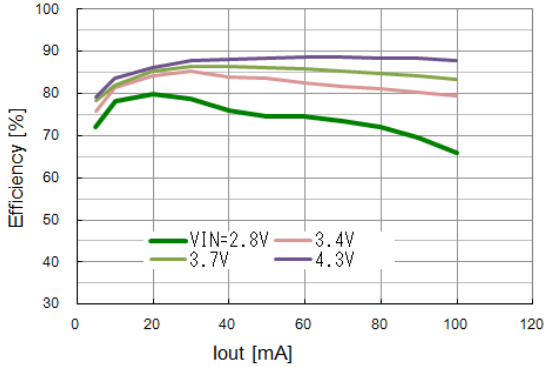
VOUT1=5.4V, VOUT2=-5.4V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=4.7uF, C_{bst}=4.7uF,
 C_{cp_cn}=2.2uF, C_{vin}=10uF+4.7uF, L=4.7uH



TYPICAL OPERATING CHARACTERISTICS

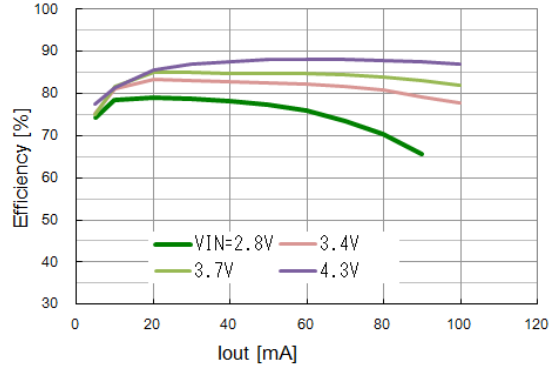
Efficiency

VOUT1=5V, VOUT2=-5V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=10uF, C_{bst}=10uF,
 C_{cp_cn}=4.7uF, C_{vin}=10uF+4.7uF, L=2.2uH



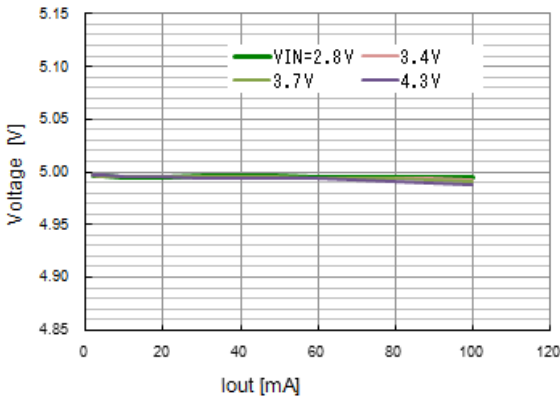
Efficiency

VOUT1=5.4V, VOUT2=-5.4V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=10uF, C_{bst}=10uF,
 C_{cp_cn}=4.7uF, C_{vin}=10uF+4.7uF, L=4.7uH



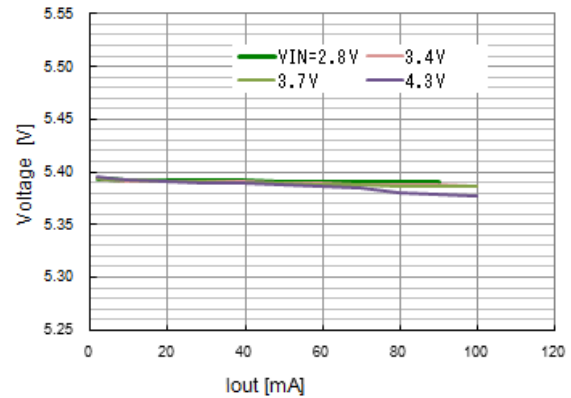
Load Regulation VOUT1

VOUT1=5V, VOUT2=-5V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=10uF, C_{bst}=10uF,
 C_{cp_cn}=4.7uF, C_{vin}=10uF+4.7uF, L=2.2uH



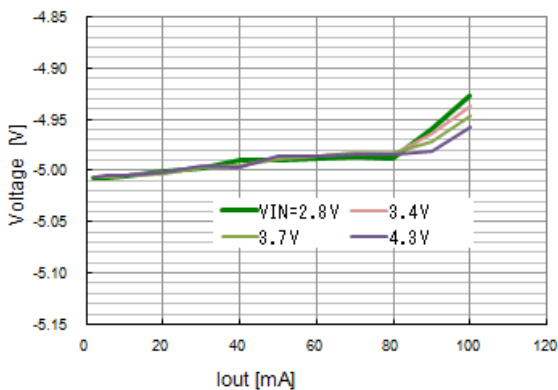
Load Regulation VOUT1

VOUT1=5.4V, VOUT2=-5.4V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=10uF, C_{bst}=10uF,
 C_{cp_cn}=4.7uF, C_{vin}=10uF+4.7uF, L=4.7uH



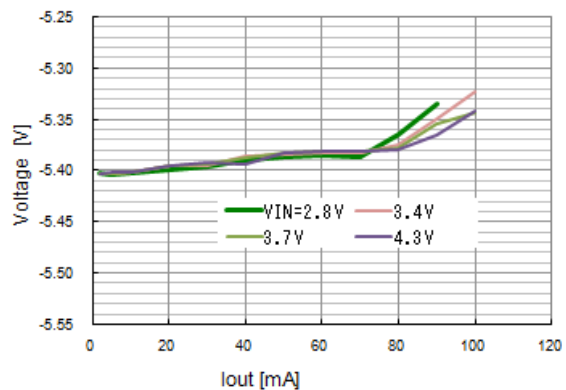
Load Regulation VOUT2

VOUT1=5V, VOUT2=-5V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=10uF, C_{bst}=10uF,
 C_{cp_cn}=4.7uF, C_{vin}=10uF+4.7uF, L=2.2uH



Load Regulation VOUT2

VOUT1=5.4V, VOUT2=-5.4V (Iout=VOUT1 to VOUT2)
 C_{vout1}=4.7uF, C_{vout2}=10uF, C_{bst}=10uF,
 C_{cp_cn}=4.7uF, C_{vin}=10uF+4.7uF, L=4.7uH



LV52130A0XA/4XA

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV52130A0XA-VH	WLP15 (1.55x2.15) (Pb-Free)	4000 / Tape & Reel
LV52130A4XA-VH	WLP15 (1.55x2.15) (Pb-Free)	4000 / Tape & Reel

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